

## CLAIM AMENDMENTS

1           1. (previously presented) A spread spectrum digital  
2 communication receiver, the receiver comprising:

3           an input memory buffer for storing samples of an input  
4 signal;

5           a code generator circuit for generating a regenerated  
6 user code;

7           a device for the estimation of a channel delay profile  
8 energy, for computing the time delays and amplitudes of each  
9 received multi-path component of said input signal;

10          a plurality of fingers; and

11          a finger allocation unit for processing said channel  
12 delay profile energy in order to select the strongest multi-path  
13 components of said input signal and allocate them to said fingers;  
14 wherein the device for the estimation of a channel delay profile  
15 energy comprises:

16          a basic correlator having a first input for sequentially  
17 reading from a memory location of said input memory buffer a  
18 plurality of samples of said input signal, a second input for  
19 receiving from said code generator circuit a regenerated user code,  
20 and an output terminal for generating, by means of a correlation  
21 operation between said plurality of samples of said input signal  
22 and said regenerated user code, a value of said channel delay  
23 profile energy; and

24           a memory controller circuit for addressing said input  
25   memory buffer so that said first input of said basic correlator is  
26   successively fed with the content of the memory locations of said  
27   memory buffer, each addressing operation corresponding to a new  
28   correlation operation of said basic correlator for the computation  
29   of a new value of said channel delay profile energy.

1           2. (previously presented) The receiver according to  
2   claim 1, wherein the values of said channel delay profile energy  
3   are progressively stored in a profile accumulation memory.

1           3. (previously presented) The receiver according to  
2   claim 2, wherein said memory controller circuit addresses said  
3   profile accumulation memory so that the reading operations of said  
4   basic correlator from said input memory buffer and the writing  
5   operations into said profile accumulation memory are handled by the  
6   memory controller circuit.

1           4. (previously presented) The receiver according to  
2   claim 3, wherein said memory controller circuit updates the  
3   addressing of said input memory buffer and said profile  
4   accumulation memory every NC chips, where NC is equal to the  
5   integration window size, changing the reading and writing positions  
6   of said basic correlator.

1           5. (previously presented) The receiver according to  
2 claim 3, wherein, when the last memory location of both said input  
3 memory buffer and said profile accumulation memory is reached, the  
4 addressing restarts circularly on a first location of both  
5 memories.

1           6. (previously presented) The receiver according to  
2 claim 3, wherein said basic correlator is time multiplexed, at a  
3 multiple of the chip frequency, between a plurality of memory  
4 locations of said input memory buffer and of said profile  
5 accumulation memory.

1           7. (previously presented) The receiver according to  
2 claim 2, wherein said delay profile energy is obtained by  
3 accumulating the energies of several delay profiles.

8 - 9. (canceled)

1           10. (previously presented) A spread spectrum digital  
2 communication receiver, the receiver comprising:  
3           a code generator circuit for generating a regenerated  
4 user code;  
5           a memory buffer for storing samples of said regenerated  
6 user code;

7           a device for the estimation of a channel delay profile  
8   energy, for computing the time delays and amplitudes of each  
9   received multi-path component of an input signal received by said  
10   receiver;

11           a plurality of fingers; and

12           a finger allocation unit for processing said channel  
13   delay profile energy in order to select the strongest multi-path  
14   components of said input signal and allocate them to said fingers;  
15   wherein the device for the estimation of a channel delay profile  
16   energy comprises:

17           a basic correlator having a first input for receiving  
18   said input signal and a second input for sequentially reading from  
19   a memory location of said memory buffer a plurality of samples of  
20   said regenerated user code, and an output terminal for generating,  
21   by means of a correlation operation between said input signal and  
22   said plurality of samples of said regenerated user code, a value of  
23   said channel delay profile energy; and

24           a memory controller circuit for addressing said memory  
25   buffer so that said second input of said basic correlator is  
26   successively fed with the content of the memory locations of said  
27   memory buffer, each addressing operation corresponding to a new  
28   correlation operation of said basic correlator for the computation  
29   of a new value of said channel delay profile energy.

1           11. (previously presented) The receiver according to  
2 claim 10, wherein the values of said channel delay profile energy  
3 are progressively stored in a profile accumulation memory.

1           12. (previously presented) The receiver according to  
2 claim 11, wherein said memory controller circuit addresses said  
3 profile accumulation memory so that the reading operations of said  
4 basic correlator from said memory buffer and the writing operations  
5 into said profile accumulation memory are handled by the memory  
6 controller circuit.

1           13. (previously presented) The receiver according to  
2 claim 12, wherein said memory controller circuit updates the  
3 addressing of said memory buffer and said profile accumulation  
4 memory every NC chips, where NC is the integration window size,  
5 changing the reading and writing positions of said basic  
6 correlator.

1           14. (previously presented) The receiver according to  
2 claim 12, wherein, when the last memory location of both said  
3 memory buffer and said profile accumulation memory is reached, the  
4 addressing restarts circularly on a first location of both  
5 memories.

1           15. (previously presented) The receiver according to  
2 claim 12, wherein said basic correlator is time multiplexed, at a  
3 multiple of the chip frequency, between a plurality of memory  
4 locations of said memory buffer and of said profile accumulation  
5 memory.

1           16. (previously presented) The receiver according to  
2 claim 12, wherein said delay profile energy is obtained by  
3 accumulating the energies of several delay profiles.

1           17. (currently amended) A method for the estimation of  
2 the channel delay profile energy in a spread spectrum digital  
3 communication receiver of the type comprising a code generator  
4 circuit for generating a regenerated user code and a memory buffer  
5 for storing samples of said regenerated user code and having a  
6 first output port for feeding a plurality of fingers with a  
7 corresponding plurality of samples of the regenerated user code and  
8 a second output port, comprising the steps of:

9           a) sequentially reading a first plurality of samples of  
10 the regenerated user code from the second output of said memory  
11 buffer;

12           b) correlating said plurality of samples of said  
13 regenerated user code with an input signal  $y(k)$  for generating a  
14 first value of the channel delay profile energy;

15           c) updating the reading position on said input memory  
16   buffer every NC chips where NC is the integration window size for  
17   reading a further plurality of samples of the regenerated user  
18   code;

19           d) correlating said further plurality of samples of said  
20   regenerated user code with said input signal for generating a  
21   further value of the channel delay profile energy, said generated  
22   value of the channel delay profile energy being stored in a profile  
23   accumulation memory; and

24           e) repeating the steps c) to d) in order to compute all  
25   the values of the channel delay profile.

1           18. (previously presented) The method according to  
2   claim 17, further comprising the step of storing each generated  
3   value of said channel delay profile energy in a profile  
4   accumulation memory.